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PTO/SB/21 (08-00) 2812

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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/527,634
Filing Date	March 17, 2000
First Named Inventor	Lo, Sun Man
Group Art Unit	2812
Examiner Name	Eron J. Sorrell
Total Number of Pages in This Submission: 10	Attorney Docket Number: 010262-013100US

ENCLOSURES *(check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☒ **Amendment / Reply**
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Assignment Papers *(for an Application)*
- ☒ **Drawing (w/ revisions, 1 sheet)**
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s)
- ☐ After Allowance Communication to Group
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ **Other Enclosure(s)** *(please identify below)*: **Return Postcard**

Remarks: The Commissioner is authorized to charge any additional fees to Deposit Account 20-1430.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm and Individual name	Townsend and Townsend and Crew LLP Paul C. Haughey Reg. No. 31,836
Signature	Paul C. Haughey
Date	December 13, 2002

CERTIFICATE OF MAILING

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PATENT

Attorney Docket No.: 010262-013100US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Examiner: Eron J. Sorrell
GLENN WEGNER ET AL.	Art Unit: 2812
Application No.: 09/527,634	
Filed: March 17, 2000	AMENDMENT
For: UART AUTOMATIC HALF-DUPLEX DIRECTION CONTROL WITH PROGRAMMABLE DELAY	

Assistant Commissioner for Patents
Washington, D.C. 20231

December 13, 2002

Sir:

In response to the Office Action mailed September 13, 2002, please amend the above-identified application as follows:

IN THE SPECIFICATION:

On page 3, please replace the paragraph beginning at line 7 with the following paragraph:

A1

--Fig. 1 is a block diagram of a UART 10. The UART includes eight channels 12. Channel 0 indicates the internal circuitry for that channel, which is not shown but would be the same for the other eight channels. In particular, it has a 64-bit transmit first in/first out (FIFO) buffer 14 and a 64-byte receive FIFO 16. The channel also includes other control circuitry and registers. The channels interface via I/O lines 18 to serial data communication lines. The data can be provided through an internal bus 20 to an internal FIFO manager 22. The FIFO manager provides the data in both directions through a second internal bus 24 to a PCI local bus interface 26. This interfaces with a PCI bus 28. Fig. 1 also shows PCI bus configuration registers 13, an EEPROM interface